

Shenzhen Fullchip Electronic Technology Co., Ltd

TX8C1260 data manual

Enhanced 8-bit general-purpose microcontroller

Rev. V2.0

Revision Record

Date	Version	Tracing
2026-10-20	V2.0	1. Optimize document formatting;
2023-07-12	V1.23	1. Modify the description of ADC reference voltage;
2023-07-05	V1.22	1. Modify the description of ADC reference voltage;
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2023-05-30	V1.20	1. Modify the description of ADC reference voltage;
2023-04-27	V1.19	1, modify the ADC internal reference description;
2023-02-03	V1.18	1. Solve the garbled code problem when some devices are opened for reading;
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2022-08-04	V1.16	1. Modify the TX8C1260SO16 package pin diagram.
2022-07-27	V1.15	1. Add TX8C1260SO16 package model.
2022-07-12	V1.14	1, Modify TX8C1260SS20 model package pin 6 Name annotation error.
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2022-06-13	V1.12	1, add TX8C1260SS28 model, modify the chip operating temperature of -40℃ ~ 105℃.
2022-06-08	V1.11	1, add LED part function description.
2022-05-30	V1.10	1. Add TX8C1260SO20 package model.
2022-05-25	V1.9	1, correct some parameters of memory characteristics.

Note:

1、The company reserves the right to the final interpretation of the functions, performance, scheme, design and improvement of all the following products.

2、The Company reserves the right to copy and change the documents.

Contents

1. Product Overview....1
1.1. Instructions....1
1.2. Features....2
1.3. Pin distribution....6
1.4. Package information....10
1.5. Package size drawing....11
1.6. Pin Instructions....14
2. MCU Electrical Parameters....19
2.1. Absolute maximum rating....19
2.2. Dc electrical characteristics....20
2.3. Ac electrical characteristics....21
2.3.1. Operating conditions at power on and power off....21
2.3.2. Built-in reset and power control module features....22
2.3.3. External clock source features....22
2.3.4. Features of the internal clock source....23
2.4. IO drive capability characteristics....24
2.5. Simulating electrical characteristics....25
2.5.1. 12-bit ADC characteristics....25
2.6. Memory characteristics....26
2.7. EMC characteristics....26
2.7.1. ESD Electrical characteristics....26
2.7.2. Latch Up electrical characteristics....27

1. Product Overview

1.1. Instructions

The TX8C1260 is a high-performance, low-power 8051 core MCU with a maximum operating frequency of 48MHz, built-in 16K byte LogicFlash memory (supporting EEPROM functions), and 2K byte SRAM.

Analog resources:

1 12-bit 500KSPS SARADC.

Timer Resources:

6 16-bit advanced timers (3 pairs of complementary PWM, with dead zone control or 6 independent PWM),

5 16-bit general purpose timers (all support Capture, Count, PWM functions),

1 16-bit wake timer (all support Capture, Count, PWM functions),

1 8-bit buzzer (support PWM, Count functions),

1 watchdog timer.

A standard communication interface:

1 SPI interface, 1 IIC interface and 2 UART interfaces (of which UART1 supports DMA working mode).

LED display function:

Supports up to 8COM x 12SEG.

GPIO:

Built-in 30K pull-down resistor, multiple drive gears configurable, each IO can be used as an input to ADC, each IO can be used as an IO interrupt wake-up port.

Support a wide range of voltage power supply, the operating voltage is 2.4V ~

5.5V (can support battery application scenarios), the operating temperature range of -40℃ ~ +105℃. A variety of power saving operating modes to ensure the requirements of low power applications, the minimum power consumption mode <5uA.

The TX8C1260 provides QFN20, TSSOP20, SSOP20, SSOP28, SOP20, SOP16, SOP8 and other package formats. The peripheral resource configuration varies according to different package formats.

Application occasions:

- Small appliances
- Toys
- E-cigarettes
- Bluetooth charging bay, wireless charge
- Covers the application of 003 series MCU products

1.2. Features

➢Kernel

- Ultra Fast 8051 core (1T)
- Instructions fully compatible with traditional 8051
- Maximum working frequency: 48MHz
- 32 interrupt sources, support hardware two-level priority
- Support for online debugging interface
- Support code encryption
- Live burning is supported

➢Operating voltage

- 2.4V ~ 5.5V Wide voltage range supply

➢Storage

- 16K byte LogicFlash memory, for storing user code, and support for class EEPROM (wipe times typical value of 100,000)
- 2K bytes of RAM

➢Clock

- Internal 1~48MHz high precision HIRC, supports calibration (error ±1%)
- Internal 64KHz low speed LIRC, supports calibration (error ±1%)
- External 32.768 KHz/8~40MHz crystal oscillator, requiring external capacitors

➢Reset

- Power on reset
- Undervoltage reset
- Reset foot reset
- Watchdog overflow reset
- LVD reset low pressure detection, provide a magnitude 8 low voltage detecting voltage (4.0/4.3 2.4/2.7 2.0/2.2 / / 3.0/3.7 / V)

➢Digital peripheral

- 1 SPI high-speed serial interface, supporting master-slave mode
- 1 I2C interface, support multi-master and slave mode
- 2 UART interfaces, maximum support 4Mbps, of which UART1 supports DMA mode

➢Timer Resources

- Six 16-bit advanced timers, support 3 pairs of complementary outputs, support dead zone insertion and event brake functions, support single pulse mode. Or support 6 independent PWM outputs
- 5 16-bit universal timers, all supporting Capture, Count, PWM functions

- 1 16-bit wake timer
- 1 8-bit buzzer timer
- 1 watchdog timer

➢LED display function

- Supports up to 8COM x 12SEG

➢High security

- Support 32-bit CRC validation to ensure data accuracy

➢Low power consumption

- Supports IDLE, STOP, and SLEEP low-power modes
- Static power consumption 5uA (@25℃, 5V power supply), 3uA(@25℃, 3.3V power supply)
- Low power wake-up time is less than 100us

➢1 high precision 12-bit analog-to-Digital Converter (ADC)

- A conversion clock supports up to 10MHz with a maximum sampling rate of 500KSPS
- Offset correction step 2mV, DNL +-2 INL +-4
- External input channel Any IO optional, 2 analog channels
- ADC effective bit about 10bit (5V voltage regulator power supply, ADC through the internal switch connected to the chip VCC, this voltage as the ADC reference voltage, ADC full scale is equal to VCC)

➢GPIO

- All ports can input and output 5V signals
- All support rising edge/falling edge/double edge interrupts
- All support up/down resistance functions
- All support wake up function

- Programmable drive capability, drive current range 4mA ~ 64mA, each gear adjustment 4mA.
- Support OD output low/high mode.
- Support independent control of the pull-down resistor, resistance value 30KΩ

➢ **High reliability**

- ESD HBM 6KV
- Latch-up ±200mA @25℃

➢ **96-bit chip Unique ID (UID)**

➢ **Package**

- TSSOP20
- SSOP20/SSOP28
- QFN20
- SOP8/SOP16/SOP20

➢ **Operating temperature range**

- -40℃ ~ +105℃

1. 3. Pin distribution

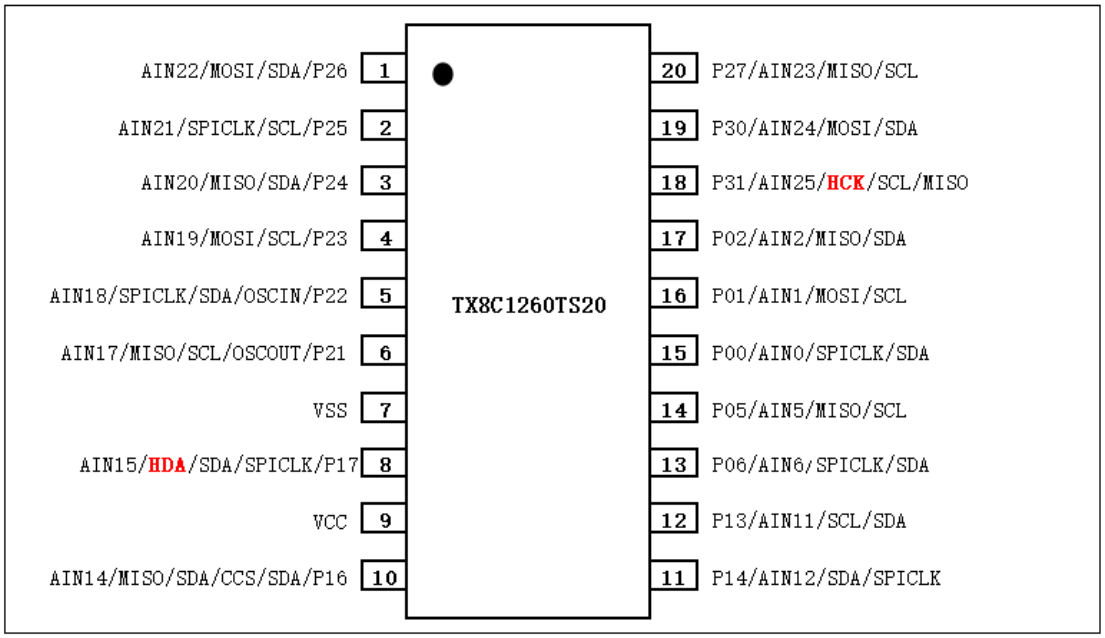


Figure 11-TX8C1260TS20 (TSSOP20) package diagram

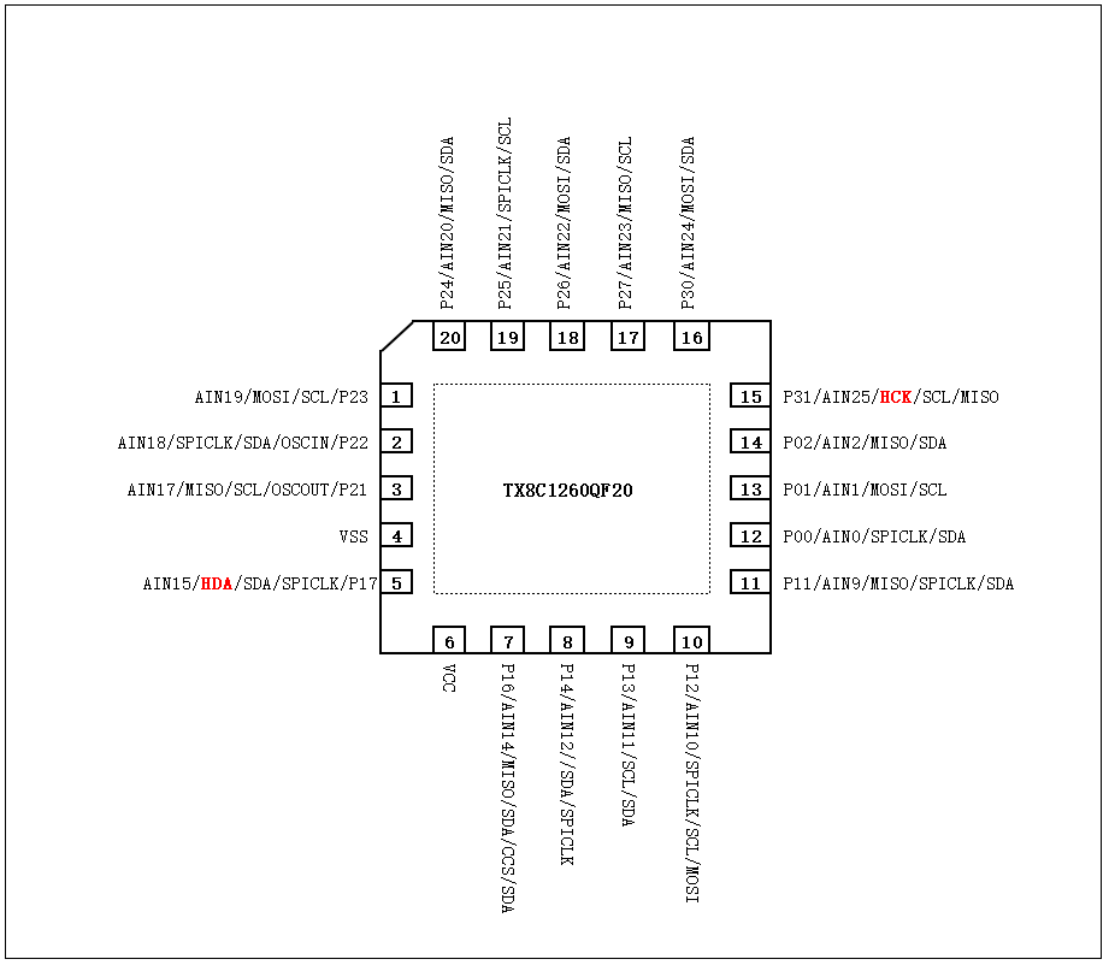


Figure 2-TX8C1260QF20 (QFN20) package diagram

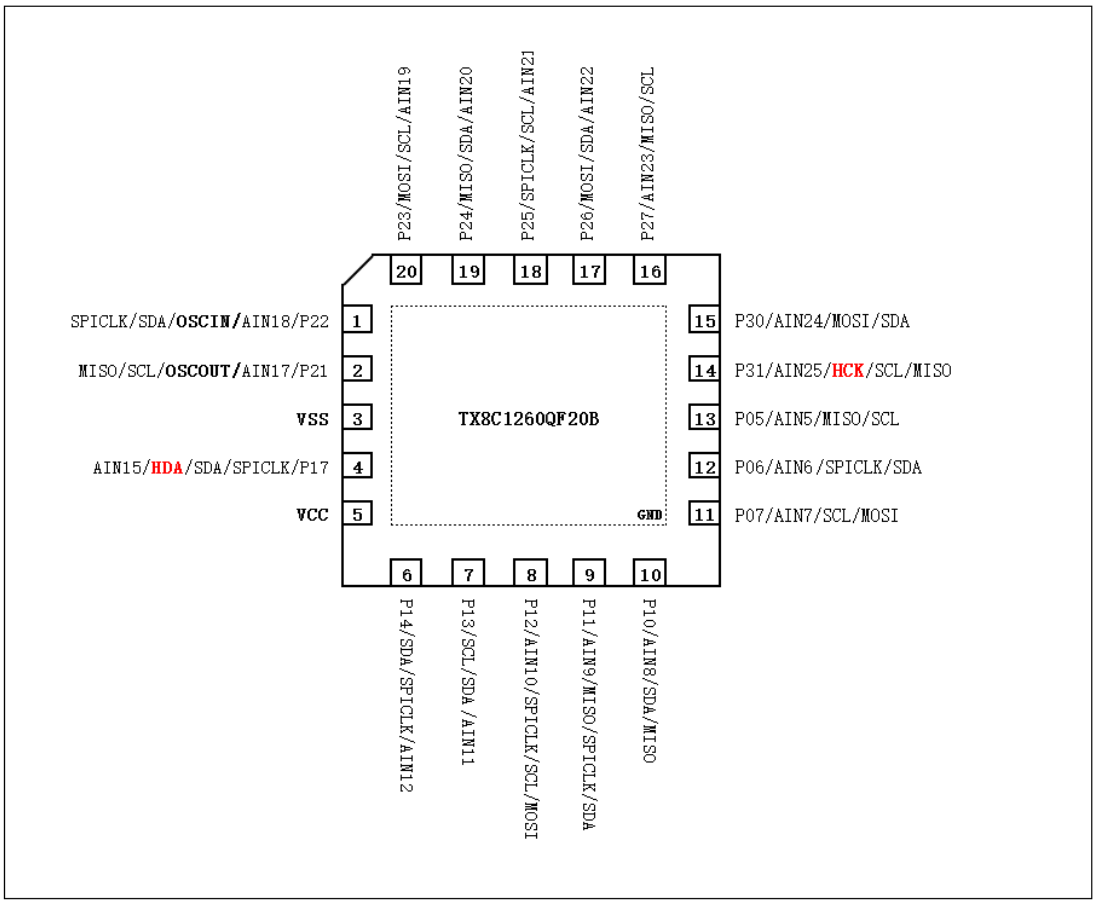


Figure 3-TX8C1260QF20B (QFN20) package diagram

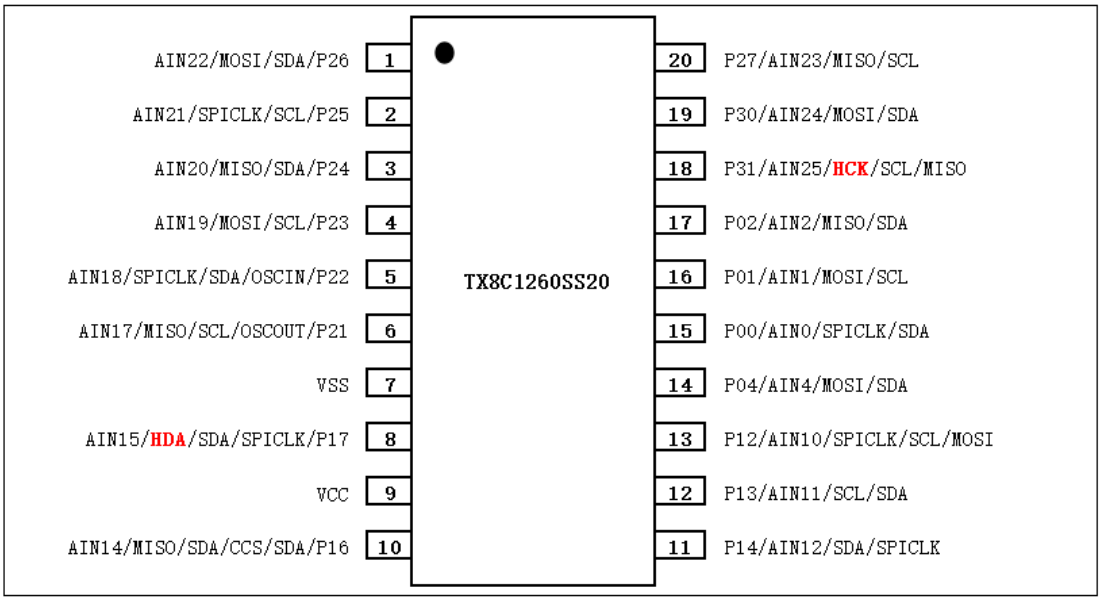


Figure 4-TX8C1260SS20 (SSOP20) package diagram

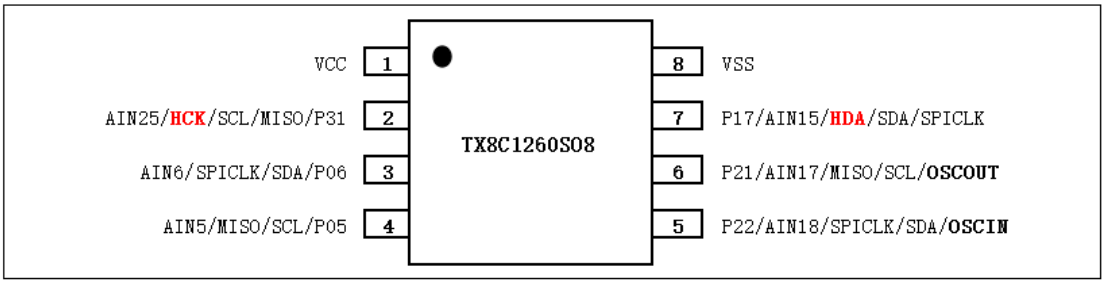


Figure 5-TX8C1260S08 (SOP8) package diagram

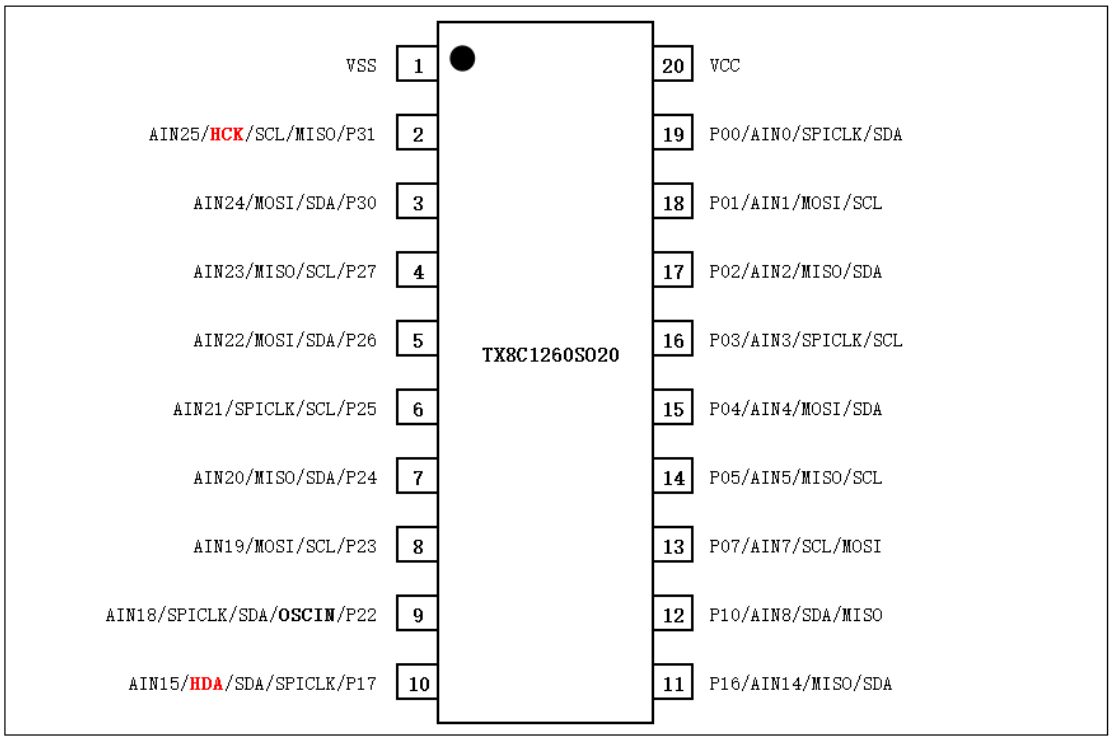


Figure 6-TX8C1260S020 (SOP20) package diagram

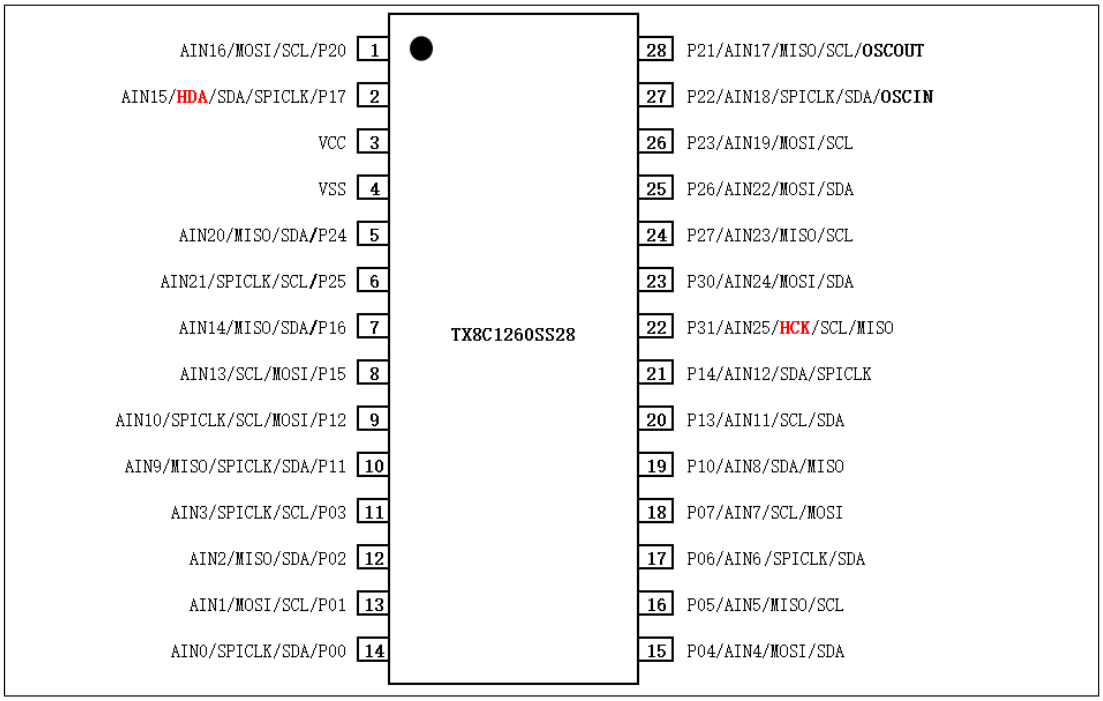


Figure 7-TX8C1260SS28 (SSOP28) encapsulation diagram

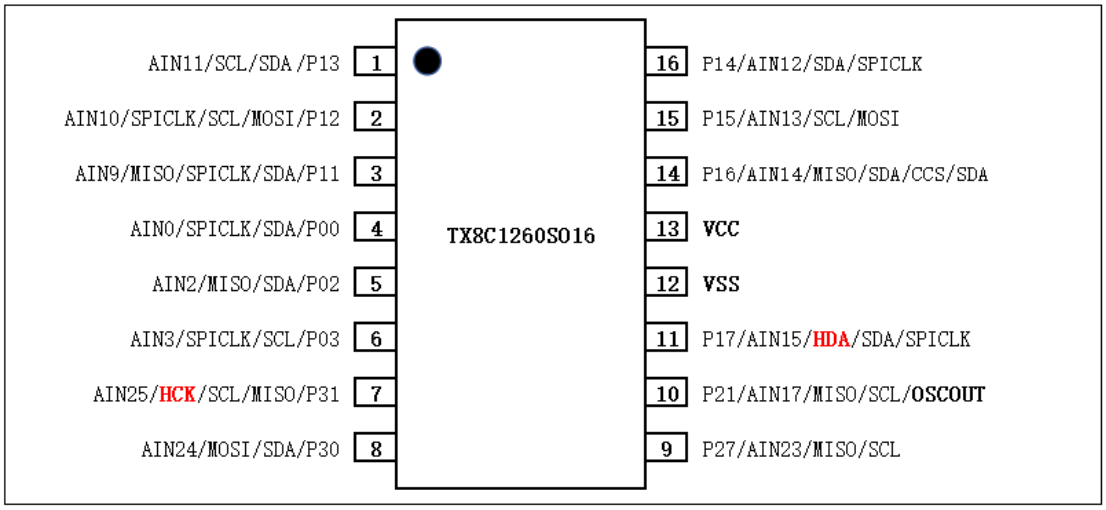


Figure 8-TX8C1260SO16 (SOP16) package diagram

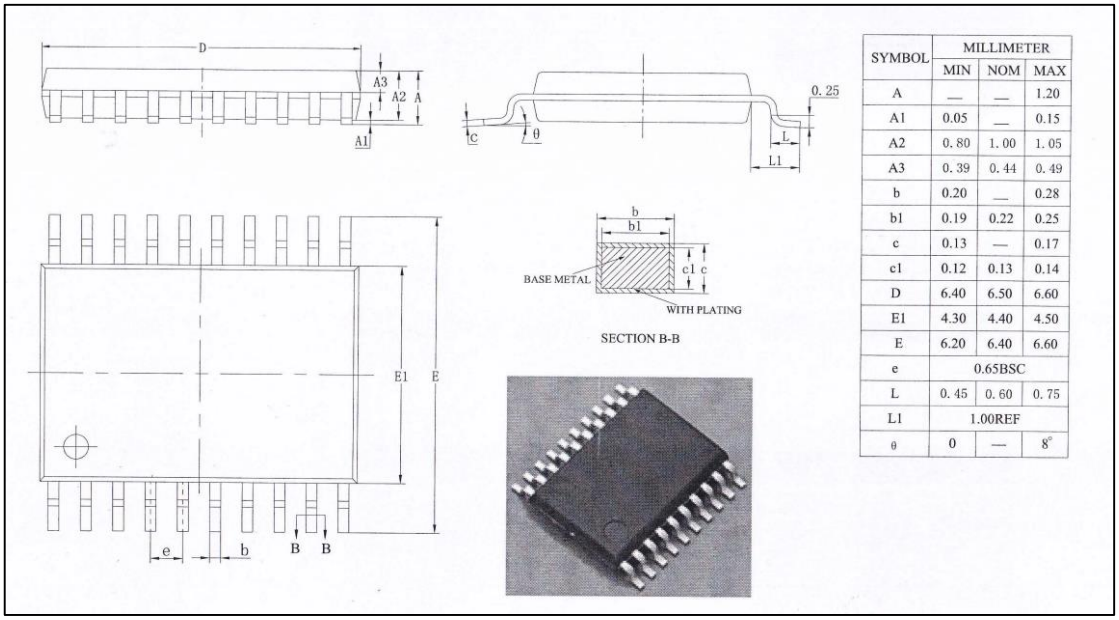
1.4. Package information

The models of the TX8C1260 series are as follows:

Model number	Package	Packaging
TX8C1260TS20	TSSOP20	Tube mount
TX8C1260QF20	QFN20	Disc mount

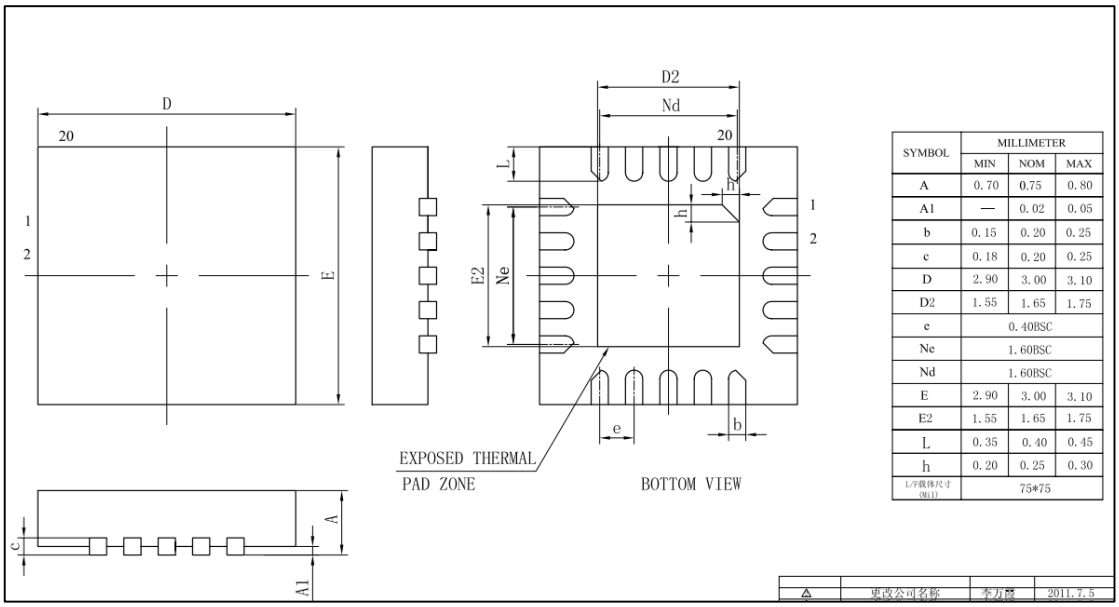
TX8C1260QF20B	QFN20	Disc mount
TX8C1260SS20	SSOP20	Tube mount
TX8C1260S08	SOP8	Tube mount
TX8C1260S020	SOP20	Tube mount
TX8C1260SS28	SSOP28	Tube mount
TX8C1260S016	SOP16	Tube mount

1.5. Package size drawing



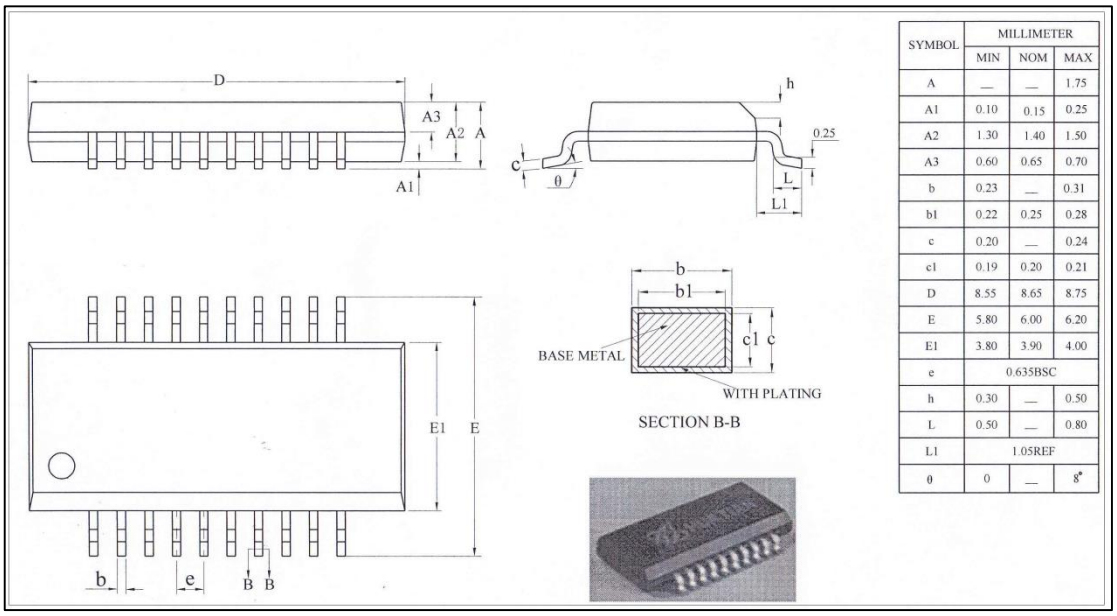
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.28
b1	0.19	0.22	0.25
c	0.13	—	0.17
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
θ	0	—	8°

Figure 9-TSSOP20 encapsulates a POD



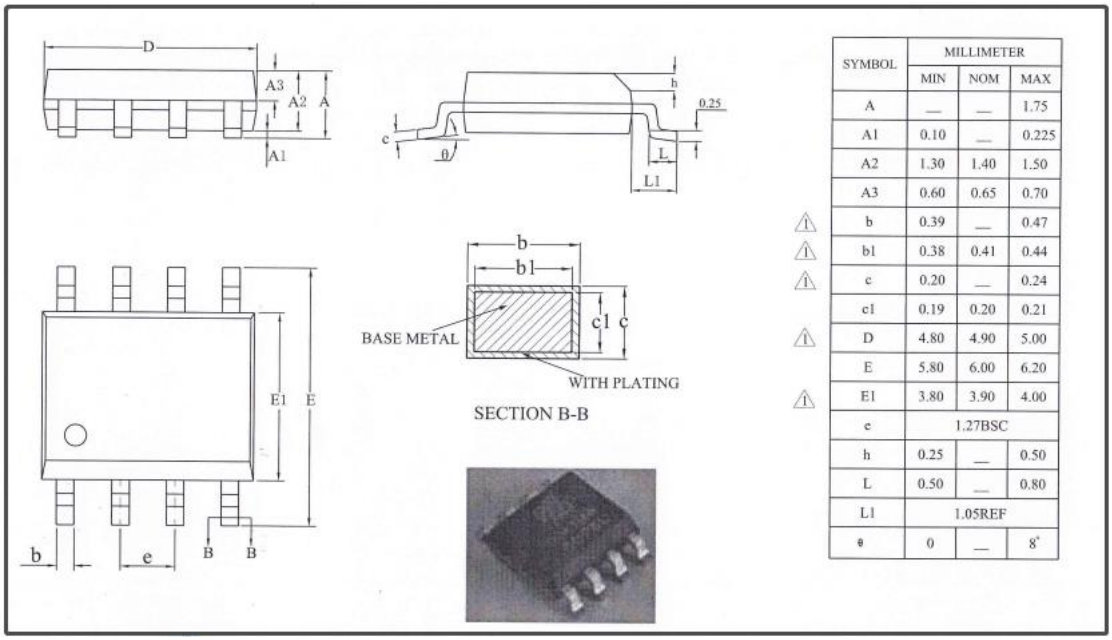
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30
L/F载体尺寸 (MIL)	75*75		

Figure 10-QFN20 encapsulating a POD



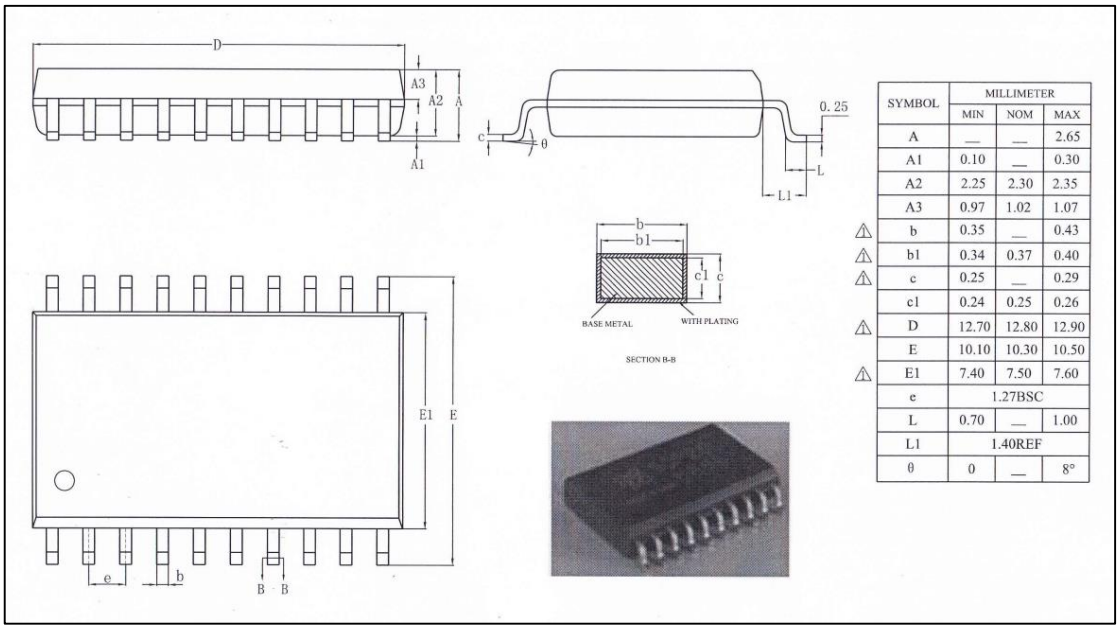
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 11-SSOP20 encapsulating a POD



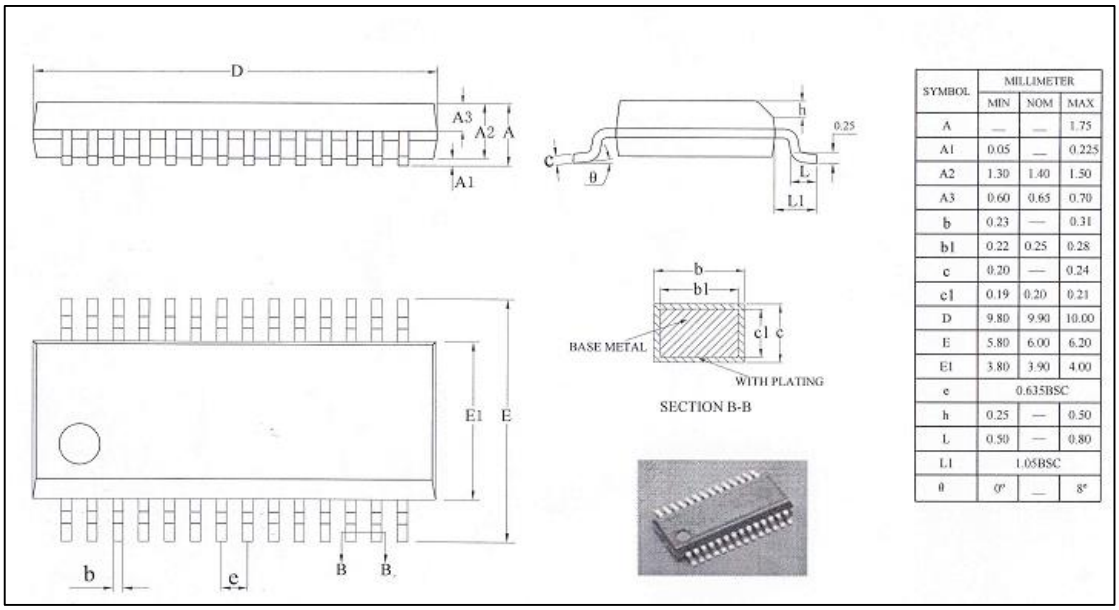
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
⚠1 b	0.39	—	0.47
⚠1 b1	0.38	0.41	0.44
⚠1 c	0.20	—	0.24
c1	0.19	0.20	0.21
⚠1 D	4.80	4.90	5.00
E	5.80	6.00	6.20
⚠1 E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 12-SOP8 encapsulating a POD



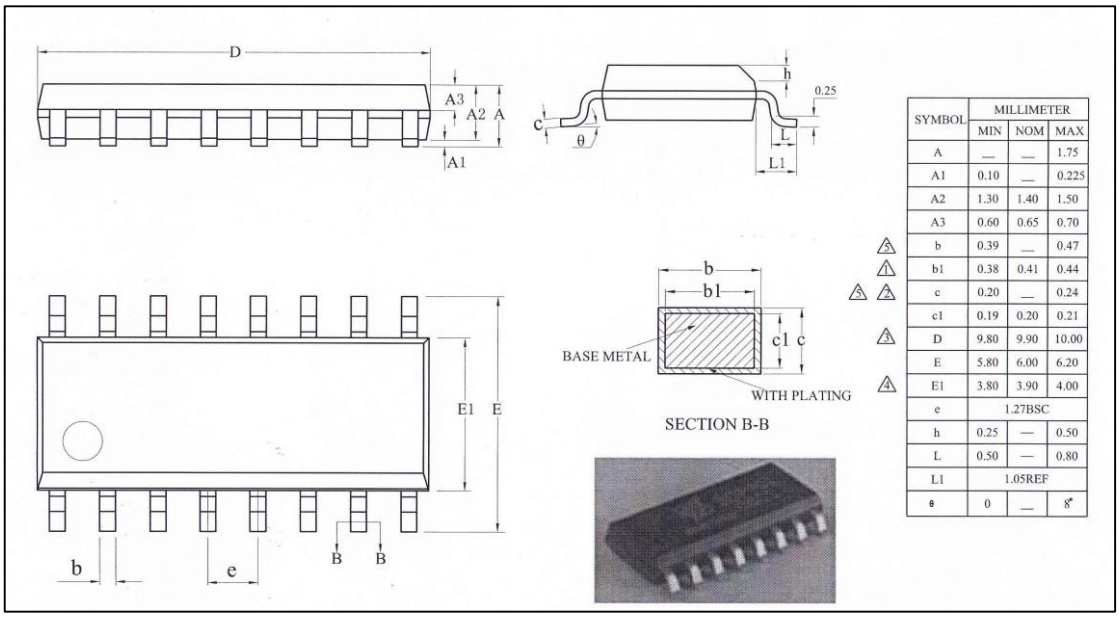
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
⚠ b	0.35	—	0.43
⚠ b1	0.34	0.37	0.40
⚠ c	0.25	—	0.29
c1	0.24	0.25	0.26
⚠ D	12.70	12.80	12.90
E	10.10	10.30	10.50
⚠ E1	7.40	7.50	7.60
e	1.27BSC		
L	0.70	—	1.00
L1	1.40REF		
θ	0	—	8°

Figure 13-SOP20 encapsulates a POD



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.05	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0°	—	8°

Figure 14-SSOP28 encapsulating a POD



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 15-SOP16 encapsulating a POD

1.6. Pin Instructions

Pin name	I/O	Function Description	Reset state	Reuse function
VCC	A	Power supply	-	There is no

GND	A	to	-	There is no
P00	I/O	P0 port Each port can be set to either input or output mode The input module can enable internal pull-up The output module can be set to open leaky output	The pin defaults to high resistance input	P00 AIN0【ADC Input Channel 0】 SPICLK【SPI CLK】
P01				P01 AIN1【ADC Input Channel 1】 MOSI【SPI MOSI】
P02				P02 AIN2【ADC Input Channel 2】 MISO【SPI MISO】
P03				P03 AIN3【ADC Input Channel 3】
P04				P04 AIN4【ADC Input Channel 4】
P05				P05 AIN5【ADC Input Channel 5】 MISO【SPI MISO】
P06				P06 AIN6【ADC Input Channel 6】 MOSI【SPI MOSI】
P07				P07 AIN7【ADC Input Channel 7】 SCL【I2C SCL】
P10	I/O	P1 port Each port can be set to either input or output mode The input module can enable internal pull-up The output module can be set	The pin defaults to high resistance input	P10 AIN8 [ADC Input Channel 8] SDA【I2C SDA】
P11				P11 AIN9【ADC Input Channel 9】 MISO【SPI MISO】
P12				P12 AIN10【ADC Input Channel 10】 SPICLK【SPI CLK】 SCL【I2C SCL】

P13		to open the leakage output		P13 AIN11【ADC Input Channel 11】 SCL【I2C SCL】 SDA【I2C SDA】 SPICLK【SPI CLK】 MOSI【SPI MOSI】
P14				P14 AIN12【ADC Input Channel 12】 SDA【I2C SDA】
P15				P15 AIN13【ADC Input Channel 13】 SCL【I2C SCL】
P16				P16 AIN14【ADC Input Channel 14】 CCS [Constant current Source Output Pin] SDA【I2C SDA】
P17				P17 AIN15 [ADC Input Channel 15] HDA【 Write debug data pin 】 SDA【I2C SDA】
P20	I/O	P2 port Each port can be set to either input or output mode The input module can enable internal pull-up The output module can be set to open leaky output	The pin defaults to high resistance input	P20 AIN16【ADC Input Channel 16】
P21				P21 AIN17【ADC Input Channel 17】 OSCOUT【 Crystal Output pin 】
P22				P22 AIN18【ADC Input Channel 18】 OSCIN【 Crystal Input Pin 】
P23				P23 AIN19【ADC Input Channel 19】 RSTB【 Reset pin 】
P24				P24 AIN20【ADC Input Channel 20】
P25				P25

				AIN21【ADC Input Channel 21】 RSTB【 Reset pin 】
P26				P26 AIN22【ADC Input Channel 22】
P27				P27 AIN23【ADC Input Channel 23】
P30	I/O	Port P3 Each port can be set to either input or output mode The input module can enable internal pull-up The output module can be set to open leaky output	P31 defaults to pull-up open, other pins default to high resistance input	P30 AIN24【ADC Input Channel 24】
P31				P31 AIN25【ADC Input Channel 25】 HCK【 Burn debug clock pin 】 SCL【I2C SCL】

Function description of pins, Table 1.5.1 is a function description table representing IO analog functions and non-arbitrary digital pins.

Table 1.5.1 - IO analog function and non-arbitrary digital pin function description table

Function Numbers	Feature name	Function description
1	AIN0~26	Analog ADC input channels 0~26
2	OSCIN/OSCOUT	External crystal oscillator input/output
3	HCK	Burn/Debug function clock input
4	HDA	Burn/debug function data input/output
5	SCL	I2C's clock
6	SDA	Data for I2C

7	SPICLK	SPI clock
8	MOSI	MOSI for SPI
9	MISO	MISO for SPI

Table 1.5.2 - IO Digital Function Arbitrary mapping function description table

Function Number	Feature name	Function description
1	UART1_TX	UART1 TX output
2	UART0_TX	UART0 TX Output
3	STMR5_PWM	Advanced Timer5 PWM output
4	STMR4_PWM	Advanced Timer4 PWM output
5	STMR3_PWM	Advanced Timer3 PWM output
6	STMR2_PWM	Advanced Timer2 PWM output
7	STMR1_PWM	Advanced Timer1 PWM output
8	STMR0_PWM	Advanced Timer0 PWM output
9	BUZ	Buzzer timer PWM output
10	WUT_PWM/CLKO	Wake Timer PWM output/clock IO output
11	TMR4_PWM	Normal Timer4 PWM output
12	TMR3_PWM	Basic Timer3 PWM output
13	TMR2_PWM	Basic Timer2 PWM output
14	TMR1_PWM	Basic Timer1 PWM output
15	TMR0_PWM	Basic Timer0 PWM output
16	TMR0_CAP	Basic Timer0 Capture input
17	TMR1_CAP	Basic Timer1 Capture input
18	TMR2_CAP	Basic Timer2 Capture input

19	TMR3_CAP	Basic Timer3 Capture input
20	TMR4_CAP0	Normal Timer4 Capture 0 input
21	TMR4_CAP1	Normal Timer4 Capture 1 Enter
22	TMR4_CAP2	Normal Timer4 Capture 2 Input
23	UART0_RX	UART0 RX input
24	UART1_RX	UART1 RX input
25	WUT_CAP	Wake up Timer Capture input
26	WKUP_IN0	IO Wake channel 0 input
27	WKUP_IN1	IO Wake channel 1 Input
28	WKUP_IN2	IO Wake channel 2 Input
29	WKUP_IN3	IO Wake channel 3 input
30	FB_IN	IO fault brake signal input
31	ADC_ETR	ADC external IO trigger signal input

2. MCU Electrical Parameters

2.1. Absolute maximum rating

Symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{VCC}	Operating voltage	-	2.4	5	5.5	V
V_{VCCA} (1)	Simulate part of the operating voltage (ADC/DAC not used)	-	2.4	5	5.5	V
	Simulate part of the operating voltage (Use ADC/DAC)	-	2.4	5	5.5	
Vpin	Pin input voltage	-	GND－0.3	-	VCC＋0.3	V
T_A	Operating temperature	-	－40	-	105	℃

T_{ST}	Storage temperature	-	- 55	-	150	℃

2.2. Dc electrical characteristics

Symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
VCC	Operating voltage	Fsys=0 to 48Mhz	2.4	5	5.5	V
V_{VCCA} (1)	Simulate part of the operating voltage (ADC/DAC not used)	Fsys=0 to 48Mhz	2.4	5	5.5	V
	Simulate part of the operating voltage (Use ADC/DAC)	Fsys=0 to 48Mhz	2.4	5	5.5	V
I_{VCC}	Normal working mode	VCC=5V, Fsys=48Mhz, All peripherals off, crystal off	-	5.38	-	mA
		VCC=5V, Fsys=24Mhz, All peripherals off, crystal oscillator off	-	3.82	-	mA
		VCC=5V, Fsys=16Mhz, All peripherals off, crystal off	-	3.30	-	mA
		VCC=5V, Fsys=8Mhz, All peripherals off, crystal off	-	2.75	-	mA
		VCC=5V, Fsys=64Khz, All peripherals off, crystal off	-	895	-	uA
		VCC=3.3V, Fsys=48Mhz, all peripherals off, crystal off	-	5.04	-	mA
		VCC = 3.3 V, Fsys = 24 MHZ, All peripherals off, crystal off	-	3.62	-	mA
		VCC=3.3V, Fsys=16Mhz, all peripherals off, crystal off	-	3.13	-	mA
		VCC = 3.3 V, Fsys = 8 MHZ, All peripherals off, crystal off	-	2.63	-	mA
		VCC = 3.3 V, Fsys = 64 KHZ, All peripherals off, crystal off	-	842	-	uA
I_{sleep}	Dormant current	VDD=5V, all peripherals shut down, IO wakes up	-	5.4	-	uA
		VDD=3.3V, all peripherals off, IO wakes up	-	3.4	-	uA

V_{IL}	Input the low-level voltage	-	VSS	-	0.3 VCC	V
V_{IH}	Input high level voltage	-	0.5 VCC	-	VCC	V
R_{PU}	Pull up equivalent resistance	-	-	25	-	K Ω
R_{PD}	Pull down equivalent resistance	-	-	25	-	K Ω
C_{IO}	Capacitance of the I/O pin	-	2.5	3	3.5	pF
V_{OL}	Output low-level voltage	No load	-	-	0.1 VCC	V
V_{OH}	Output high level voltage	No load	0.9 VCC	-	-	V

2.3. Ac electrical characteristics

2.3.1. Operating conditions at power on and power off

Working conditions for power on and power off:

Symbols	Parameters	Conditions	Minimum	Maximum	Units
t_{VCC}	V_{VCC}	T_A = 27 ° C	5	-	Mu s
t_{VCCA}	V_{VCCA}		5	-	

Power-on and power-off status:

Chip status	Power on			Power down	
	Power-on protection	Power-on reset	Working properly	Low power reset	Power down reset
Power supply voltage (in V)	< 1.8	1.8-2.4	> 2.4	< 1.85	< 1.65
System power consumption (uA)	< 0.2	> 300	Power on normally, power consumption is determined by the system clock frequency and peripherals	Material 300	< 0.2

2.3.2. Built-in reset and power control module features

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
VCC_{PVD}	Programmable voltage detector for level selection	LVDCON0[4:2]=0x0, power failure detection threshold/power on detection	-	1.85/2.05	-	V
		LVDCON0[4:2]=0x1, power failure detection threshold/power on detection	-	2.05/2.25	-	V
		LVDCON0[4:2]=0x2, power failure detection threshold/power on detection	-	2.25/2.45	-	V
		LVDCON0[4:2]=0x3, power failure detection threshold/power on detection	-	2.50/2.75	-	V
		LVDCON0[4:2]=0x4, power failure detection threshold/power on detection	-	2.80/3.10	-	V
		LVDCON0[4:2]=0x5, power failure detection threshold/power on detection	-	3.40/3.70	-	V
		LVDCON0[4:2]=0x6, power failure detection threshold/power on detection	-	3.85/4.20	-	V
		LVDCON0[4:2]=0x6, power failure detection threshold/power on detection	-	4.15/4.50	-	V
$V_{PVDhyst}$ (2)	VCC hysteresis	-	-	-	-	mV

Note: The above data is from the chip performance acceptance test and is not tested in production.

2.3.3. External clock source features

Low speed crystal oscillator characteristics:

Symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
f_{xoscm}	User external low speed clock frequency	-	-	32.768	-	KHz
V_{BIAS}	XOSCI/XOSCO bias level	-	-	770	-	mV
V_{xoh}	XOSCI Input pin high voltage	-	-	975	-	mV
V_{xol}	XOSCO input pin low voltage	-	-	525	-	mV
$Duty_{(xoscm)}$	Duty cycle	-	42	-	58	%
I_L	Low speed clock power consumption	-	-	1.5		uA
ACC_{xoscm}	HSE accuracy	-	-	-	-	ppm

$t_{SU(xoscm)}$	Starting time	-	-	2	-	s

High speed crystal oscillator characteristics:

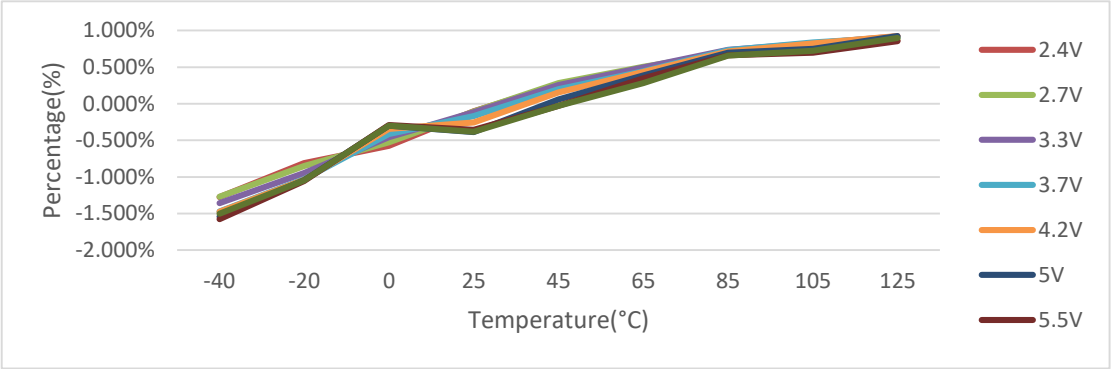
Symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
f_{xoscm}	User external high speed clock frequency	-	4	16	40	MHz
V_{BIAS}	XOSCI/XOSCO bias level	-	-	770	-	mV
V_{xoh}	XOSCI Input pin high voltage	-	-	975	-	mV
V_{xol}	XOSCO input pin low voltage	-	-	525	-	mV
$Duty_{(xoscm)}$	Duty cycle	-	42	-	58	%
I_L	High speed clock power consumption	-	-	350	-	uA
ACC_{xoscm}	HSE accuracy	-	-	-	-	ppm
$t_{SU(xoscm)}$	Starting time	-	-	5	-	ms

2.3.4. Features of the internal clock source

HIRC Oscillator characteristics:

Symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{VCCA}	Supply voltage	-	2.4	5.0	5.5	V
f_{HRC}	Frequency	Test after trim at 25℃ (accuracy	-	48	-	MHz
ACC_{HSI} (3)	Accuracy of the HSI oscillator	-40 ° C to 85 ° C	-	-	-	%
$t_{SU(HSI)}$	HSI oscillator startup time	-	-	60	-	us
$I_{VCCA(HSI)}$	HSI oscillator power consumption	Average power consumption	-	1.1	-	mA

The following figure shows the test values of 48MHz HIRC at full temperature conditions and full voltage range:

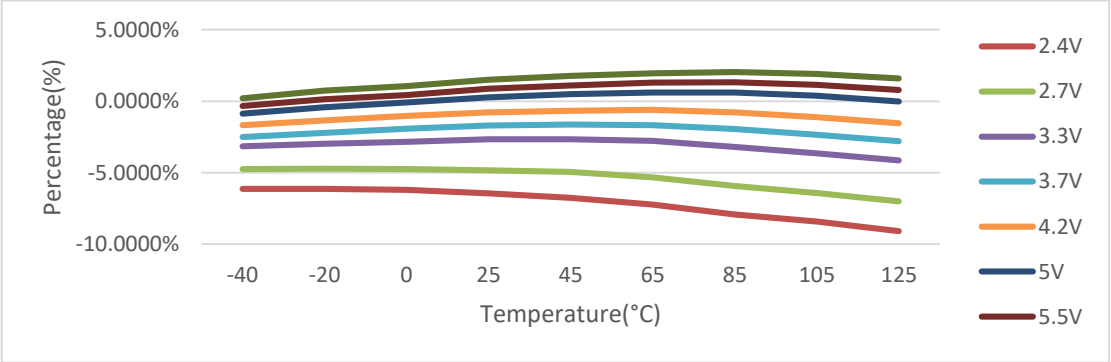


Percentage of HIRC full temperature range deviation

LIRC oscillator characteristics:

Symbol	Parameters	Conditions	Minimum	Typical value	Maximum value	unit
f_{LRC}	Frequency	TA=25℃	-	64	-	kHz
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	0.5	-	uA

Below is the test value of the 64KHz LIRC at full temperature conditions and full voltage range:



Percentage of LIRC full temperature range deviation

2.4. IO drive capability characteristics

symbol	Parameters	Conditions	Minimum	Typical	Maximum value	Units
IO	IO port push current	VCC 5V power supply, IO drive capability configuration gear	-	2.5	-	mA
		VCC 5V power supply, IO drive capability configuration gear,	-	50	-	mA
		VCC 3.3V power supply, IO drive capability configuration gear	-	1	-	mA

		VCC 3.3V power supply, IO drive capability configuration gear	-	25	-	mA
IO	IO port perfusion current	VCC 5V power supply, IO drive capability configuration gear	-	9	-	mA
		VCC 5V power supply, IO drive capability configuration gear	-	125	-	mA
		VCC 3.3V power supply, IO drive capability configuration gear	-	4.5	-	mA
		VCC 3.3V power supply, IO drive capability configuration gear	-	70	-	mA

2.5. Simulating electrical characteristics

2.5.1. 12-bit ADC characteristics

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{VCCA}	Supply voltage	-	2.8	5.0	5.5	V
I_{VCCA} (1)	Current consumption	VCCA acts as a reference	-	360	-	uA
f_{ADC}	ADC Clock Frequency	-	-	-	9.6	MHz
Fconv	Conversion Rate	-	-	-	480	KHz
R_{AIN} (2)	External input impedance	-	-	-	-	Kohm
C_{ADC} (2)	Internal sampling and holding	-	-	-	-	pF
t_{STAB} (2)	Power-on time	-	-	-	1000	us
t_{conv} (2)	Sampling time	-	5	-	256	Tclk
ENOB (3)	Significant digits (The reference	-		10		Bit

Note: (3) The input/output frequency of IO near the ADC input signal is not higher than 10KHz; The reference voltage of the ADC is VCC and the full scale is VCC; ENOB 10bit is the test result obtained under the power supply of 5V regulator, which will be affected by the power supply deviation and lead to the loss of accuracy in practical application, and the performance of the

significant bit 10bit cannot be guaranteed under other voltage;

2.6. Memory characteristics

Symbols	Parameters	Conditions	Minimum	Typical value	Maximum value	Units
V_{prog}	Programming voltage	-	2.8	5.0	5.5	V
t_{prog}	Byte programming time	-	-	160	-	us
t_{RC}	Read operation time	-	38	-	70	ns
t_{ERASE}	Page erase time	-	-	100	-	ms
t_{ME}	Whole chip erase time	-	-	100	-	ms
I_{DD}	Supply current	Read mode (@25MHz)	3.7	-	4.5	mA
		Write Pattern	-	8	-	mA
		Erase mode	-	9	-	mA
NEND	Life span (number of erases)	Wipe and write 100,000 times in 105℃ high	-	10	-	Ten thousand times
t_{RET}	Data retention period	After wiping 100,000 times at room temperature,	-	10	-	years

2.7. EMC characteristics

2.7.1. ESD Electrical characteristics

Symbol	Parameters	Test conditions	Maximum value	Units	Grades
ESD	Electrostatic discharge (Human Discharge	TA = + 25℃, JEDEC EIA/JESD22-A114	6000	V	-
	Electrostatic discharge (Component Charging	TA = + 25℃, JEDEC EIA/JESD22-C101-B	1000	V	-

2.7.2. Latch Up electrical characteristics

Symbols	Parameters	Test condition	Type of test	Minimum value	Units
LU	Static latch-up class	JEDEC STANDARD NO.78D NOVEMBER 2011	Class I (TA = +25 ℃)	+ 200	mA